UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,399	03/01/2004	Chi-Yang Lin	VIAP0100USA	2398

27765 7590 05/01/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,399	LIN ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are pending and have been examined.

2. Claims 1-13 are rejected.

Response to Arguments

3. Applicant's arguments filed March 16, 2006 have been fully considered but they are not persuasive. In response to applicant's argument that Baxter is nonanalogous art (i.e., since the memory 39 is not used to connect additional peripheral devices), it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Baxter teaches a system and method of reducing latency in transferring data to a memory device while applicant's invention is drawn to a system and method for reducing latency in transferring data to an I/O port. Both applicant and Baxter teach a multiplexer connected between two bridges to reduce the access latency to an expansion device, thus applicant and Baxter solve the same particular problem.

Drawings

4. The drawings were received on March 16, 2006. These drawings are acceptable.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 and 11-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Peleg et al. (US006557065B1) further in view of Baxter, III (US006813689B2).

For claim 1 AAPA discloses:

An SOC (Fig. 1, 41) comprising:

- a processor for controlling operation of the SOC (Fig. 1, 32);
- a high-speed bridge circuit connected to the processor (Fig. 1, 34), the high-speed bridge circuit being used to control signal transmission between the processor and a high-speed peripheral device (Fig. 1, 38) connected to the high-speed bridge circuit (AAPA; [0005]);
- a low-speed bridge circuit connected to the high-speed bridge circuit (Fig. 1, 36), the low-speed bridge circuit being used to control signal transmission between the high-speed bridge circuit and a first low-speed peripheral device (Fig. 1, 42) connected to the low-speed bridge circuit (AAPA; [0005]);

While AAPA discloses a SOC for use in an embedded system (Fig. 1, 30) it does not disclose further connecting the SOC to an external bridge for expanding the connectivity of the embedded system.

Peleg teaches an embedded system (Fig. 4) that consists of an SOC (Fig. 4, 400) comprising a processor for controlling the operation of the SOC (col. 5, ll. 32-53), a graphics processor, and a Northbridge (functions much like the high-speed and low-speed bridges of AAPA). The SOC further comprises an expansion port (not shown, however it is the pins of the SOC 400 that connect to the bus 12) for connecting to the expansion bridge circuit (i.e., "Southbridge Chip", Fig. 4, 30). The Southbridge is responsible for controlling signal transmission between the SOC and low-speed peripheral devices (such as printers, modems, keyboards, mice, CD-ROM drives, hard disk drives...col. 1, line 31- col. 2, line 8).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to connect a Southbridge chip like that of Peleg to a System On a Chip (SOC) like that of AAPA such the functionality and expandability of the embedded system is greatly increased.

While AAPA in view of Peleg teaches an SOC connected to a Southbridge (i.e., expansion bridge circuit) they do not expressly state where Southbridge connects to the internal components of the SOC. Peleg shows as prior art that Southbridge circuits are normally connected to Northbridge circuits (Fig. 1 and 2). Applied to AAPA it appears as though the Southbridge would connect to the low-speed bridge circuit since the Southbridge provides access to additional low speed devices. It would be beneficial to provide a connection between the Southbridge chip and the SOC such that both high-speed devices attached to the high-speed

bridge circuit and low-speed devices attached to the low-speed bridge circuit are given fast access to the additional devices attached to the Southbridge.

Baxter teaches a system (Fig. 2C) that shows a processor 40 connected to a bus 36 that also connects to two bridges 37 and 43. The two bridges are similar to the high-speed and low-speed bridge circuits of AAPA in view of Peleg in that they control access to devices attached to their subordinate buses. Assuming for sake of example that the Mem controller & I/O Bridge 37 represents the high-speed bridge circuit of AAPA in view of Peleg while the I/O Bridge 43 represents the low-speed bridge circuit. It is clearly demonstrated that the two bridges are connected and they control access to their attached devices (devices 10 and 17). Baxter then contemplates the proper placement of another device Memory 39 that requires fast-access by not only processor 40 but also the devices 10 and 17. The proper placement of the memory 39 is equivalent to the placement of the expansion port (i.e., Southbridge) of AAPA in view of Peleg. By attaching the Southbridge to the low-speed bridge circuit access by the CPU is negatively affected because the CPU needs to go through both the high-speed and low-speed bridge circuits. Likewise, attaching the Southbridge to the high-speed bridge circuit negatively affects access by devices attached to the low-speed bridge since the requests must traverse not only the low-speed bridge but must also go through the high-speed bridge circuit. Baxter provides a solution to this problem in the form of a multiplexer (Fig. 2C, 38).

Baxter teaches a multiplexer (Fig. 2C, 38) for connecting bridges 37 and 43 along with devices 10 and 17 to an additional memory device 39. Had the memory device 39 been connected

directly to bus 35 access from devices 10 would result in a two "hop" lag because the transaction would need to traverse both I/O Bridge 43 and Mem controller & I/O Bridge 37. A similar situation exists if the memory device 39 was attached only to bus 34. By placing multiplexer 38 between buses 34 and 35 data moved from bus 34 to bus 35 (and vice versa) and data moved between devices attached to buses 34 and 35 (including devices 10 and 17 and bridges 37 and 43) experience less latency because only one hop is needed to transfer data (col. 6, ll. 23-59). Therefore by connecting the Southbridge (as taught by Peleg) to both the high-speed bridge and the low-speed bridge (as disclosed by AAPA) through a multiplexer (as taught by Baxter) the delay required to moved data to and from the Southbridge is reduced.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to connect the Southbridge of Peleg to the both the high-speed and low-speed bridge circuits of AAPA through a multiplexer like that of Baxter such that the delay required to move data from the Southbridge to various embedded system components is reduced.

For claim 2:

The SOC of claim 1 wherein the processor comprises a RISC processor (AAPA; [0005]).

For claim 3:

The SOC of claim 1 further comprising: a multiplexer comprising (Baxter; Fig. 2C, 38):

- an input connected to the expansion port (the port to which the Southbridge of Peleg will attach);

- a first output connected to the high-speed bridge circuit; and a second output connected to the low-speed bridge circuit (as noted above...by connecting the Southbridge (as taught by Peleg) to both the high-speed bridge and the low-speed bridge (as disclosed by AAPA) through a multiplexer (as taught by Baxter) the delay required to moved data to and from the Southbridge is reduced).

For claim 4:

The SOC of claim 3 wherein the multiplexer connects the input and the first output when the expanding bridge circuit is connected to the expansion port (as noted above...by connecting the Southbridge (as taught by Peleg) to both the high-speed bridge and the low-speed bridge (as disclosed by AAPA) through a multiplexer (as taught by Baxter) the delay required to moved data to and from the Southbridge is reduced).

For claim 5:

The SOC of claim 3 wherein the expansion port is selectively connected to an input/output port of the SOC or to the expanding bridge circuit (as noted above...by connecting the Southbridge (as taught by Peleg) to both the high-speed bridge and the low-speed bridge (as disclosed by AAPA) through a multiplexer (as taught by Baxter) the delay required to moved data to and from the Southbridge is reduced).

For claim 6:

The SOC of claim 5 wherein the multiplexer connects the input and the second output when the expansion port is connected to the input/output port (as noted above...by connecting the Southbridge (as taught by Peleg) to both the high-speed bridge and the low-speed bridge (as disclosed by AAPA) through a multiplexer (as taught by Baxter) the delay required to moved data to and from the Southbridge is reduced).

For claim 7:

The SOC of claim 1 wherein the low-speed bridge circuit is connected to a first input/output port (AAPA; Fig. 1, 44), and the expanding bridge circuit is connected to a second input/output port (Peleg; Fig. 4, ports connecting to buses 72 and 82); wherein the first input/output port is used to connect to the first low-speed peripheral device (AAPA; [0005]), and the second input/output port is used to connect to the second low-speed peripheral device (Peleg; col. 1, line 31- col. 2, line 8).

For claim 8:

The SOC of claim 1 wherein the expansion port is connected to the expanding bridge circuit using a bus connector (Peleg; Fig. 4, 12).

For claim 11:

The SOC of claim 1 wherein the expanding bridge circuit comprises a south bridge circuit of x86 architecture (Peleg; col. 1, line 31 – col. 2, line 8).

For claim 12:

The SOC of claim 1 wherein the SOC is installed in a package, and the expansion port comprises a plurality of pinouts of the package (AAPA; [0005-0006]).

For claim 13:

The SOC of claim 1 wherein the SOC is utilized in an embedded system (AAPA; [0005]).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Peleg et al. (US006557065B1) further in view of Baxter, III (US006813689B2) as applied to claim 8 above, and further in view of "DFI Excitedly Introduces Dual Specification Motherboard Adpoting VIA KT266/DDR¢wAD72".

8. As previously discussed above AAPA in view of Peleg teaches a SOC with a bus connection to an expansion bridging circuit (Southbridge). The Southbridge circuit enables the SOC to increase the functionality and expandability of the embedded system. Baxter teaches that by connecting the Southbridge to both the high-speed and low-speed bridging circuits through a multiplexer that the delay required to move data from the Southbridge to various embedded system components is reduced. However, neither AAPA nor Peleg nor Baxter teach the specific protocol used to connect the high-speed/low-speed bridging circuits to the expanding bridge circuit (Southbridge).

In the article titled, "DFI Excitedly Introduces Dual Specification Motherboard Adpoting VIA KT266/DDR¢wAD72" it is taught that simply by using the V-link interconnect bus to connect the Northbridge to the Southbridge the bandwidth is increased by 100% (page 2) to an amazing 266MB per second.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the bus connection between the high-speed and low-speed bridging circuits and the expansion bridge circuit as a V-link interconnect in order to increase the bandwidth by 100% over typical prior art interconnects.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Peleg et al. (US006557065B1) further in view of Baxter, III (US006813689B2) as applied to claim 8 above, and further in view of what was commonly known at the time of applicant's invention as evidenced by Klein (US 5,935,226).

As previously discussed above AAPA in view of Peleg teaches a SOC with a bus connection to an expansion bridging circuit (Southbridge). The Southbridge circuit enables the SOC to increase the functionality and expandability of the embedded system. Baxter teaches that by connecting the Southbridge to both the high-speed and low-speed bridging circuits through a multiplexer that the delay required to move data from the Southbridge to various embedded system components is reduced. However, neither AAPA nor Peleg nor Baxter teaches the

specific protocol used to connect the high-speed/low-speed bridging circuits to the expanding bridge circuit (Southbridge).

The Examiner respectfully submits that it was well known at the time of applicant's invention to use a PCI bus to connect the Northbridge (the combination of the high-speed and low-speed bridging circuits) to the Southbridge as evidenced by Klein. Klein teaches as a matter of prior art (Fig. 1) that a Southbridge **30** is typically connected to the PCI bus **26** of the Northbridge **24**.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the bus connection between the high-speed and low-speed bridging circuits and the expansion bridge circuit as a PCI bus because it was a widely accepted Northbridge to Southbridge interconnect as evidenced by Klein.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nsame discloses a system-on-a-chip structure pertinent to applicant's invention.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

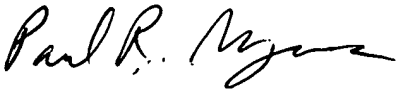
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PAUL R. MYERS
PRIMARY EXAMINER

RMS